SPI   Serial Peripherial Interface

MASTER

SLAVE

MISO

Master RX-Schieberegister n bits **in**

Eingänge

Eingänge laden, wenn load = '1'

Master TX-Schieberegister n bits **out**

MOSI

load
in Slave Schieberegister n bits **out**

SCLK

SCLK

SS#
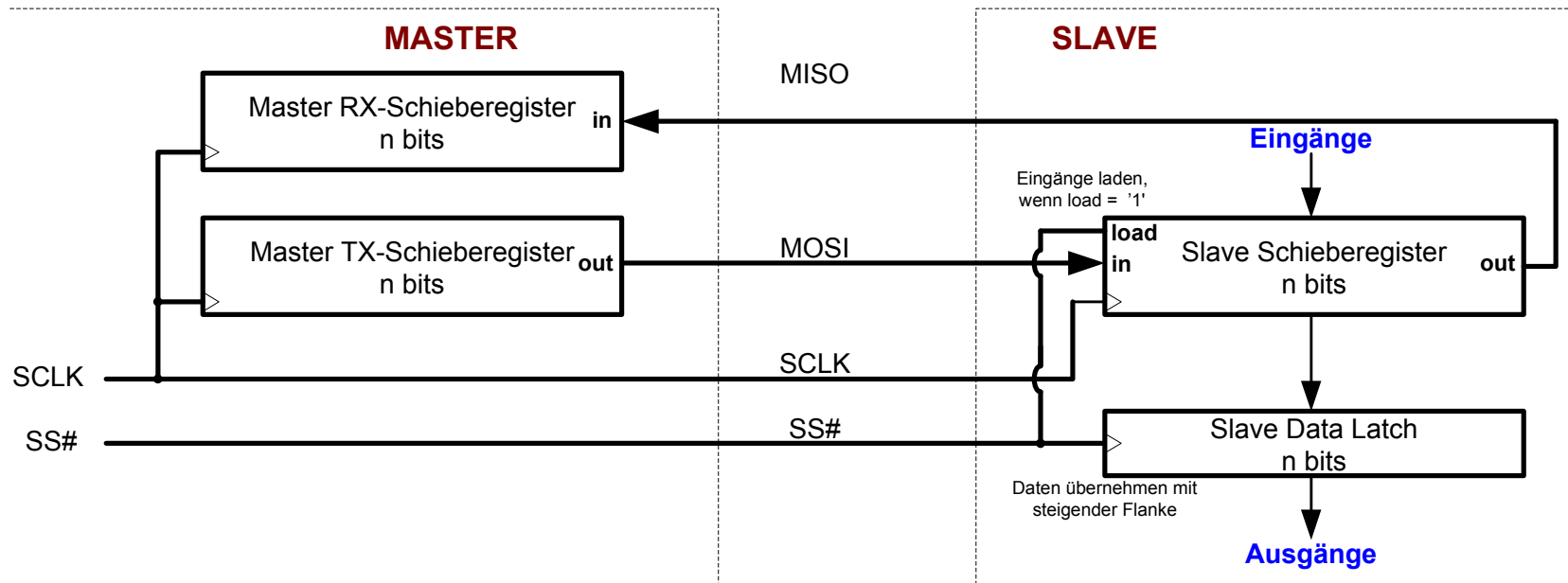
SS#

Slave Data Latch n bits

Daten übernehmen mit steigender Flanke

Ausgänge

MISO = Master In, Slave Out
MOSI = Master Out, Slave In

SCLK = Clock, erzeugt vom Master
SS#   = Slave Select, low-aktiv, erzeugt vom Master

Clock Phase CPHA

sample   shift   sample   shift

CPOL = 0

CPHA = 0 | **CPHA = 1**

shift   sample   shift   sample

CPOL = 0

Mode 0

Clock Polarity CPOL

Mode 1

Daten

Daten

CPOL = 1

Mode 2

Mode 3

CPOL = 1

Master
SCLK
MOSI
MISO
SS1#
SS2#
SS3#

Slave 1
SCLK
MOSI
MISO
SS#

Slave 2
SCLK
MOSI
MISO
SS#

Slave 3
SCLK
MOSI
MISO
SS#

MOSI = Master Out, Slave In

MISO = Master In, Slave Out

SCLK = SPI Clock

SS#   = Slave Select, low-aktiv